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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,784	03/30/2004	Chien-Chao Huang	67,200-1289	5209

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TUNG & ASSOCIATES
838 W. Long Lake Road, Suite 120
Bloomfield Hills, MI 48302

EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,784	HUANG, CHIEN-CHAO	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-18,22-31 and 35-41* is/are rejected.

7)☒ Claim(s) *8-10, 19-21, 32-34, 42-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 13, 24 and 35 are objected to because of the following informalities: inconsistent term, i.e. "a dielectric insulating layer (claim 1, line 3; claim 13,line 5; claim 24, line 3 and claim 35, line 3) versus "first dielectric insulating layer" (claim 1, lines 9-10; claim 13, line 12; claim 24 lines 5 and 8 and claim 35, line 5); "conductive portion (claim 1, lines 3-4) versus "conductive area" (claim 8, line 1). Appropriate correction is required.

In addition, in claim 1 (line 11), claim 13 (line 13), changing "the portion" into – the portion **overlying the dielectric insulating layer** – is suggested for clarity.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 24, at lines 7-9, it recites " an AlCu interconnect comprising a second barrier layer disposed on the AlCu via and over the first dielectric insulating layer." The foregoing limitations are not consistent with what has been presented in Fig. 1D, in which the second barrier layer 33A disposed on the AlCu **interconnect 32A and 32B**, instead of the AlCu via (i.e. the vertical portion filled in the via 26A).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 7, 24, 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Dixit et al (US 6,355,558).

In re claims 1 and 7, Dixit et al., in Figs. 1-4D and related text, teach a method of forming a multi-level semiconductor device wiring interconnect structure comprising the steps of:

- forming a dielectric insulating layer 26 over a conductive portion 24 (Fig.1);
- forming a via opening 34 in closed communication with the conductive portion 24 (Fig. 1);
- forming a barrier layer 44 comprising TiN to line the via opening 34 (Fig.2B);
- forming a layer of AlCu 50 to fill the via opening 34 to form an AlCu via 50 including a portion overlying the dielectric insulating layer 26 (Fig.2E); and
- forming the portion to form an AlCu interconnect line (i.e. the horizontal portion of AlCu 50 overlying the dielectric insulating layer 26 (Fig.2E).

In re claims 24 and 31, Dixit et al, in Fig.2E, teach a multi-level wiring interconnect structure for a semiconductor device comprising:

- a dielectric insulating layer 26 over a conductive portion 24;

- a AlCu via 50 (i.e. the portion resides in the via 34) comprising a barrier layer 44 (i.e. TiN) formed in the dielectric insulating layer 26 in closed communication with the conductive portion 24; and
- an AlCu interconnect line (i.e. the horizontal portion of AlCu 50 overlying the dielectric insulating layer 26) comprising a second barrier layer 56 (TiN) over the dielectric insulating layer 26 (Fig.4A).

In re claim 30, Dixit et al. also teach that the via openings are formed in an aspect ratio greater than 1.5 (col. 8, lines 33-37).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3-4, 13-15, 22-23 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dixit et al. in view of Zhou et al. (US 6,376,353).

In re claims 3 and 13, Dixit et al. do not expressly disclose that the AlCu layer 50 is formed by a magnetron sputtering carried out at a temperature less than about 400 °C.

Zhou et al. teach using the magnetron sputtering for depositing Al-Cu layer for obtaining a good adhesion property (col. 11, lines 32-34 and col. 12, lines 7-8), wherein the temperature is about 25 to 500°C (col. 11, lines 36-37), which covers the claimed range of less than about 400 °C.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use the magnetron sputtering technique, as taught by Zhou et al., for depositing the Al-Cu layer of Dixit et al., since by doing so it would form an Al-Cu layer having a good adhesion property.(col. 12, lines 7-8, Zhou et al.)

In re claims 4 and 15, Zhou et al. also remedy the deficiency in Dixit et al. because Zhou et al. teach that the pressure in the magnetron sputtering is about 0.1 to 10,000 mTorr (col. 11, line 35), which covers the claimed range of less than about 5 mTorr.

In re claims 14, 25, 26, one of the ordinary skill in the art would have been motivated to repeat the processing steps in order to form multi-level metallization layers as many as three or more as desired.

In re claims 22-23, 27, one of the ordinary skill in the art would have been motivated to repeat the processing steps in order to form multi-level metallization layers consisting essentially of AlCu wiring as many as three or more as desired.

8. Claims 5-6, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dixit et al. (US '795) in view of Chang et al. (US 6,159,842).

Dixit et al. do not teach using a FSG for the dielectric insulating layer.

Chang et al. teach using a FSG for dielectric insulating layer 16 in adjacent to a AlCu layer 14.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use the dielectric insulating consisting essentially of FSG, as taught by Chang et al., as the dielectric insulating layer of Dixit et al., since by this manner it would provide a good protection for the AlCu layer (col. 23, lines 48-50, Chang et al.).

9. Claims 2, 11, 12, 35-37 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dixit et al. in view of Matsubara et al. (US 2004/0000719).

In re claim 2, Dixit et al. do not expressly teach repeating steps a) through e) to sequentially forma an overlying AlCu via followed by an overlying AlCu interconnect line.

Matsubara et al., in an analogous art of forming a multi-level metallization, teach forming a dielectric insulating layer 12/13 over a conductive portion 11a; forming a via opening in closed communication with the conductive portion 11a; forming a barrier layer 14 to line the via opening; and forming a layer of AlCu 17 to fill the via opening to form an AlCu via and interconnect line 14/17 (Fig.14A). Matsubara et al. further teach repeating the similar processing steps to form a desired multi-level interconnect (paragraph [0135]).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to apply the approach of Matsubara et al. in Dixit et al. by repeating the processing steps of the formation of the via and interconnect line, since by this manner it would form a desired multi-level interconnect structure.

In re claims 11, 35-37, one of the ordinary skill in the art would have been motivated to repeat the processing steps in order to form multi-level metallization layers as many as three or more as desired.

In re claim 12, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to comprehend that the multi-level semiconductor device consisting essentially of AlCu wiring because each level metallization consisting essentially of AlCu (i.e. layer 50 in Dixit). By repeating layer 50 (i.e. AlCu), it would form multi-layers semiconductor device consisting essentially of AlCu.

In re claim 41, Dixit et al. teach that the barrier layer is TiN.

10. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dixit in view of Zhou et al. as applied to claim 13 above, and further in view of Chang et al.

In re claim 16, Dixit et al. in view of Zhou et al. do not teach using a FSG for the dielectric insulating layer.

Chang et al. teach using a FSG for dielectric insulating layer 16 in adjacent to a AlCu layer 14.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use the dielectric insulating consisting essentially of FSG, as taught by Chang et al., as the dielectric insulating layer of Dixit et al. in view of Zhou, since by this manner it would provide a good protection for the AlCu layer (col. 23, lines 48-50, Chang et al.).

In re claim 17, Dixit et al. also teach that the via openings are formed in an aspect ratio greater than 1.5 (col. 8, lines 33-37).

In re claim 18, Dixit et al. teach that the barrier layer is TiN.

11. Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dixit et al. in view of Matsubara et al. and further in view of n view of Chang et al.

In re claims 38 and 39, Dixit et al. in view of Matsubara et al. do not teach using a FSG for the dielectric insulating layer.

Chang et al. teach using a FSG for dielectric insulating layer 16 in adjacent to a AlCu layer 14.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use the dielectric insulating consisting essentially of FSG, as taught

by Chang et al., as the dielectric insulating layer of Dixit et al. in view of Matsubara, since by this manner it would provide a good protection for the AlCu layer (col. 23, lines 48-50, Chang et al.).

In re claim 40, Dixit et al. also teach that the via openings are formed in an aspect ratio greater than 1.5 (col. 8, lines 33-37).

Double Patenting

12. Claim 26 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 25. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Allowable Subject Matter

13. Claims 8-10, 19-21, 32-34 and 42-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither teaches nor suggests that the conductive portion comprises silicide electrical contact areas comprising a CMOS transistor portion.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

June 11, 2005

HSIEN-MING LEE
PRIMARY EXAMINER

6/11/05